

As the three-month shortened statutory period for reply is due July 14, 2004, this Response is therefore considered timely filed.

AMENDMENTS

In the Claims

Please amend the claims as follows:



PENDING CLAIMS AND STATUS THEREOF

1. (currently amended) A method for processing shadow register array control instructions, comprising:

fetching and decoding a shadow register array control instruction with a processor;

executing the shadow register array control instruction on data stored in a source array of registers to write the data from the source array of registers to a destination array of registers within one processor cycle, whereby the shadow array control instruction configured to provide provides a fast context save during interrupt and non-interrupt processing.

- 2. (original) The method according to claim 1, wherein the shadow register array control instruction is a first shadow array control instruction.
- 3. (original) The method according to claim 2, wherein the source array of registers is a primary register array and the destination array of registers is a shadow register array.
 - 4. (original) The method according to claim 3, further comprising:

 detecting that an interrupt condition has occurred.
 - 5. (original) The method according to claim 4, further comprising:

 loading the first shadow register array instruction into an instruction register for execution, the first shadow array instruction provided as a first instruction in an interrupt service routine (ISR) for an interrupt servicing the interrupt condition.

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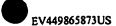
6. (original) The method according to claim 1, wherein the shadow register array control instruction is a second shadow array control instruction.

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- 7. (original) The method according to claim 2, wherein the source array of registers is a shadow register array and the destination array of registers is a primary register array.
 - 8. (original) The method according to claim 7, further comprising: detecting that an interrupt condition has occurred.
 - 9. (original) The method according to claim 8, further comprising:

 executing remaining instructions in an ISR for an interrupt servicing the interrupt condition, the remaining instructions including a return from the ISR routine, wherein an automatic context save option in the return from the ISR routine is disabled.
- 10. (original) The method according to claim 9, wherein the second shadow register array control instruction is executed before the execution of the return from the ISR routine.
- 11. (currently amended) A processor for performing shadow register array control instructions, comprising:
 - an array of primary registers for storing data;
 - an array of shadow registers for storing data;
 - a program memory for storing instructions including a shadow register array control instruction;
 - a program counter for identifying current instructions for processing; and
 - a shadow register array control logic for executing the shadow register array control instruction on a data stored in a source array of registers to write the data from the

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source array of registers to a destination array of registers within one processor cycle, whereby the shadow register control instruction configured to provide provides a fast context save during interrupt and non-interrupt processing.

- 12. (original) The processor according to claim 11, wherein the shadow register array control instruction is a first shadow array control instruction.
- 13. (original) The processor according to claim 12, wherein the source array of registers is the array of primary registers and the destination array of registers is the array of shadow registers.
 - 14. (original) The processor according to claim 12, further comprising: interrupt logic for detecting that an interrupt condition has occurred.
 - 15. (original) The processor according to claim 14, further comprising:

 an instruction register for loading the first shadow register array control instruction for execution, the first shadow array instruction provided as a first instruction in an interrupt service routine (ISR) for an interrupt servicing the interrupt condition.
- 16. (original) The processor according to claim 11, wherein the shadow register array control instruction is a second shadow array control instruction.
- 17. (original) The processor according to claim 11, wherein the source array of registers is the array of shadow registers and the destination array of registers is the array of primary registers.





- 18. (original) The processor according to claim 16, further comprising: interrupt logic for detecting that an interrupt condition has occurred.
- 19. (original) The processor according to claim 18, further comprising:

 an execution unit for executing remaining instructions in an ISR for an interrupt servicing the interrupt condition, the remaining instructions including a return from the ISR routine, wherein an automatic context save option in the return from the ISR routine is disabled.
- 20. (original) The processor according to claim 19, wherein the second shadow register array control instruction is executed before the execution of the return from the ISR routine.